Amendments to the Specification

Please replace the paragraph beginning on page 2, line 23 with the following amended paragraph:

In the aspect of the present invention to achieve the above object, there is provided a circuit for detecting an abnormal operation of memory comprising: a delay circuit for delaying an output data of the memory for a predetermined period of time and for outputting this data as a delay data; and a comparison circuit for outputting a noncoincidence ~~an incoincidence~~ signal in case that the output data of the memory and the delay data are not coincident with each other after compared.

Please replace the paragraph beginning on page 3, line 28 with the following amended paragraph:

Fig. 1 is a block circuit diagram showing the structure of the first embodiment of the present invention. An address signal output 122 from a CPU 100 is input to an address input terminal of a flash memory 101. Then the data [[to be]] stored in the input address in the flash memory 101 is respectively input as a data signal 123 to a data input terminal of the CPU 100, to an input terminal D of a first data latch 103 and to an input terminal of a delay circuit 102. The data signal 123 input to the delay circuit 102 is output as a delay circuit output 124 delayed for a predetermined period of time, and is input to the input terminal of a second data latch 104.

Please replace the paragraph beginning on page 4, line 16 with the following amended paragraph:

On the other hand, a latch signal 121 from the CPU 100 is respectively input to a latch signal input terminal G of the first data latch 103, to a latch signal input terminal G of the second data latch 104 and to an output control terminal OE (Outlet Enable) of the comparator 106. Each of the data latch ~~signal 125~~ 103 and the [[delay]] data latch ~~signal 126 holds~~ 104 hold the latched ~~value in~~ values at the rising of the latch signal 121 [[in]] at an H section of the latch signal 121. On the other hand, the latched data [[latch]] signal 123 [[125]] and the latched delay circuit output 124 are ~~data latch signal 126~~ output as the data latch signal [[123]] 125 and the delay data latch signal 126 respectively ~~circuit output 124~~ at [[that]] the time ~~through in~~ of an L section of the latch signal 121.

Please replace the paragraph beginning on page 4, line 27 with the following amended paragraph:

At each timing of the rising of latch signal 121 to be input to the output control terminal OE, the comparator 106 outputs a logical signal "L" if the signal at the input terminal A equals to the one at the input terminal B, and outputs a logical signal "H" as ~~an incoincidence~~ a noncoincidence signal 127 if the signal at the input terminal A does not equal to the one at the input terminal B. Then the ~~incoincidence~~ noncoincidence signal 127 from the comparator 106 is input to an input terminal CK of a D-FF 107. A

power source 128 from a power source VDD 110 is connected to an input terminal D of the D-FF 107. And then an abnormality detecting signal 130 turning into "H" state in detecting an abnormality is output from an output terminal Q of the D-FF 107, which is connected to an external output terminal 108. Also, a reset signal 129 from the external ~~output~~ input terminal 109 is connected to a reset input terminal R of the D-FF 107. And then when the reset signal 129 is input from the external ~~output~~ input terminal, the abnormality detecting signal 130 returns to "L" state (Fig. 1).

Please replace the paragraph beginning on page 5, line 20 with the following amended paragraph:

The flash memory 101 outputs the data signal 123 at a timing t_1 after a certain period of time (access time; $(t_1 - t_0)$), from receiving the address signal 122 from the CPU 100 with the starting point set at "t_0". The CPU 100 downloads the data of the data signal 123 at a timing t_3 at which the latch signal 121 turns into "H" state, and processes the data in the CPU 100, based on a predetermined program (Fig. 2).

Please replace the paragraph beginning on page 5, line 27 with the following amended paragraph:

The data signal 123 is delayed for a period of time $(t_2 - t_1)$ in the delay circuit 102 and is output as the delay circuit output 124. The data signal 123 and the delay circuit output 124 are respectively compared in the comparator 106 via the first data latch 103

and the second data latch 104. If they [[are]] coincide with each other at the timing t_3 at which the latch signal 121 rises to turn into "H" state, the ~~incoincidence~~ noncoincidence signal 127 remains "L" state (Fig. 2).

Please replace the paragraph beginning on page 6, line 5 with the following amended paragraph:

However, if the access time of the flash memory 101 is delayed and the output of the data signal 125 ~~misses~~ is at a timing t_5 without being output ~~outputting~~ at a timing t_4 after receiving the address signal 122, the delay circuit 102 cannot output the data [[by]] signal 124 at a timing t_6 at which the latch signal 121 rises to "H" state and the comparator 106 judges there to be noncoincidence ~~incoincident~~, to turn the noncoincidence ~~incoincidence~~ signal 127 into "H" state (Figs. 1 and 3).

Please replace the paragraph beginning on page 6, line 12 with the following amended paragraph:

If there is a rising edge at which the noncoincidence ~~incoincidence~~ signal 127 turns into "H" state, the D-FF 107 downloads the "H" data at the input terminal D connected to the power source VDD 110 and an abnormality detecting signal 130 is turned from "L" state into "H" state. Then it is notified to the outside that the output of the external output terminal 108 connected to the output terminal Q of the D-FF 107 turns from "L" state into "H" state and that the access time of the flash memory has

changed (been delayed), in other words, the abnormal operation of the flash memory 101 (Figs. 1 and 3).

Please replace the paragraph beginning on page 6, line 30 with the following amended paragraph:

According to the first embodiment as described above, the access speed of the data signal is high enough to match the timing to use in the CPU, however, it is monitored whether the noncoincidence ~~incoincidence~~ will occur or not by giving a predetermined period of delay and by comparing the data before and after the delay with each other. In other words, by checking whether the margin for delay is always saved with regard to the timing for the CPU to download the data signal, it can be detected that the access speed in the flash memory begins to become lowered for some reasons when the noncoincidence ~~incoincidence~~ occurs, though there is an enough amount of margin in an initial state. Consequently, we can learn of an abnormality before an error occurs in the integrated circuit of the micro-computer and the like in which a flash memory is built ~~operates abnormally~~, to prevent abnormal operation due to a wrong data signal with the access speed further lowered.

Please replace the paragraph beginning on page 8, line 22 with the following amended paragraph:

In referring to an address judged to be ~~incoincident~~ noncoincident during the

interruption process, the address latched by the address latch 205 [[in]] at the rising of the NAND output 232 of the latch signal 221 and of an inversion signal 231 of the abnormality detecting signal 230, remains latched during the period when the abnormality detecting signal 230 is in "H" state. Therefore, the address can be read out via the data bus 212. After finishing the execution of the interruption process, the reset signal 229 is output from the interruption control circuit 211. And then the D-FF 207 becomes reset, and the abnormality detecting signal 230 returns to "L" state from "H" state (Figs. 4 and 5).